Yield Aware Inter-logic-layer Communication in 3-D ICs: Early Design Stage Recommendations

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***Abstract*—3-D ICs provide more logic space by introducing a multiple tier structure. Through silicon vias (TSVs) are utilized for signal propagation between multiple tiers. However, TSVs are vulnerable to fracture, which leads to lower yield. This paper analyzes different yield aware TSV redundancy techniques from a hardware overhead and effective redundancy perspective. A set of mathematical relationships is derived to obtain a first-order approximation of effective redundancy and hardware design overhead. One of the results indicates that for 250 inter-tier TSV signals, the hardware overhead for 3x3 router based redundancy technique is about 3 times more than 1:4 TSV redundancy technique, while providing 5 times more effective redundancy per cell. Such results provide an early design stage estimate for the ASIC designer. We applied our proposed technique to clock domain crossing (CDC) interfaces.**

Keywords—TSV; 3-D IC; CDC

I. INTRODUCTION

3-D IC technology has provided more logic density by allowing more components to be added in smaller area. It resulted in reduction of timing constraints and provided means to integrate systems designed in different dies, even using different process technologies [1]. But 3-D ICs are subject to various challenges as well. These include an increment in temperature gradients, due to difficulty in inserting heat sinks to inaccessible layers, which also poses difficulties to clock distribution network and design for testability in 3-D ICs [2] [3] [4].

The vertical interconnects in 3-D ICs are special conductors that can pass through the silicon substrate and are called through silicon via (TSV). TSVs are vulnerable to fracture, which in turn lead to lower yield [5] [6]. To improve the yield of 3-D ICs, researchers have proposed various TSV redundancy techniques [7] [8] [9]. The overall improvement in yield for 3-D ICs is directly related to the ratio of the signal carrying TSVs to the available redundant TSVs. This research provides tools for 1st order TSV estimation, to utilize TSVs smartly. We provided a mathematical relationship to obtain effective redundancy and hardware design overhead. To the best of our knowledge, this analysis is a first attempt to obtain an early design stage estimate of the cost of hardware versus effective redundancy, to improve yield, for various numbers of signals. It is found that when signals are more uniformly spread across the TSV cells, then the effective redundancy improves. We also applied our findings on clock domain crossing techniques, as a case study, and it is found that router based redundancy provides best effective redundancy per cell, leading to best yield expectations, at the expense of higher number of TSVs and hardware complexity.

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The rest of paper is organized as follows: Section II gives an overview of TSV redundancy techniques, Section III presents our proposed yield aware TSV cell management. Section IV shows analysis of effective TSV redundancy against hardware overhead, whereas Section V provides a case study on clock domain crossing (CDC) in 3-D ICs. Finally, Section VI concludes this paper.

II. TSV REDUNDANCY TO IMPROVE YIELD

In order to minimize the footprint of redundant TSVs several different techniques have been proposed in literature [7] [8] [9]. These techniques have different levels of failure tolerance at the expense of design complexity. Before providing the details of these techniques, Fig. 1 illustrates different symbols that have been used in Fig. 2(a-c) related to TSV redundancy. Next sub-sections utilize these symbols to provide an overview of different TSV redundancies.

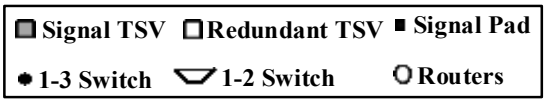


Figure 1. Various symbols used in Fig. 2

A. 1:4 TSV Redundancy Technique[7]:

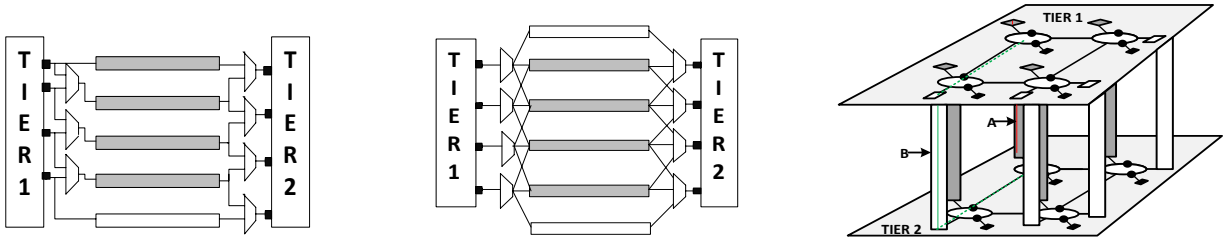
This redundancy technique adds one extra TSV for group of four TSVs, as shown in Fig. 2(a). One: 4 TSV redundancy technique can tolerate up to one TSV failure within a group of four signal carrier TSVs (as shown in Fig. 2a). In this configuration, if a TSV fails then the signal corresponding to that failed TSV is shifted to the next neighboring TSV and this arrangement is propagated until it reaches the spare TSV.

B. 2:4 TSV Redundancy [8]:

Another TSV redundancy technique is based upon 2:4 allocation, where each group of four signals has two redundant TSVs as shown in Fig. 2(b). The shaded TSVs are used under normal circumstances. If one of the two top signal TSVs fails then it is re-routed through the top redundant TSV and in case one of the bottom two signal TSVs fails then it is re-routed through the bottom TSV. This technique can tolerate up to two failures in the group of four TSVs.

C. Router Based TSV Redundancy [9]:

Router based redundancy approach, shown in Fig. 2(c), is proposed in [9]. It is called router based redundant TSV due to the involvement of routers in redundant path allocation. This technique is different from earlier two techniques as it is based on the premise that if one TSV fails then the likelihood of the failure of neighboring TSV would also increase. So instead of



(a) 1:4 TSV redundancy [7] (b) 2:4 TSV redundancy [8] (c) Router base redundancy [9]

Figure 2. Different TSV redundancy techniques for 4-bit transfer

routing failed TSV signal to a neighboring TSV, it re-routes path to a distant TSV.

Router based redundant TSV allocation for four bits transfer is illustrated in Fig. 2(c). In case TSV A fails then this redundancy re-routes the data to TSV B, which is not neighboring to TSV A. Obviously, the added resilience is obtained at the expense of more delay and overhead in hardware. Addition of extra hardware also leads towards more area, power and energy consumption.

III. YIEDL AWARE TSV CELL MANAGEMENT FOR 3-D IC: ASIC DESIGN PERSPECTIVE

In a standard cell library based application specific integrated circuit (ASIC) designs, it is desirable that TSV redundancy architectures, shown in Fig. 2, are used as one cell in the library. This section investigates each of the above mentioned redundant TSV technique from the ASIC design perspective.

A. 1:4 TSV Redundancy:

In a standard cell library-based ASIC design, TSV redundancy architecture shown in Fig. 2(a) can be used as one cell in the library. The following analysis explains how many of such 1:4 TSV redundancy cells are required to transfer X number of signals across the tiers. For example, if total X signals need to be sent from tier 1 to tier 2 using such cells, then the total cell requirement for X signals using 1:4 TSV redundancy architecture can be written in the form of (1).

$$\textit{1:4 TSV Cells Required}= N=\left\lceil \frac{X}{4} \right\rceil \tag{1}$$

Each cell of 1:4 TSV redundancy has at least one spare TSV to provide an alternate route. It can be observed that when all four available signal TSVs are not in use then this cell contains more than one redundant TSV. In case, where each 1:4 TSV redundancy cell has Y total number of signal TSVs, redundant TSVs per cell (Red_I) can be expressed as (2).

$$Red_I = 5 - Y \tag{2}$$

Similarly, for N (an integer number) 1:4 TSV redundancy cells average $Red_I/cells$ can be calculated using (3):

$$\textit{Average } Red_I/cell= \frac{\sum_{i=1}^{N}(Red_i)}{N} \tag{3}$$

However, (3) does not provide information on how well redundancy spread in different cells. For example, if one of the two 1:4 TSV cells have only one redundant TSV and the other cell has 4 redundant TSV, on average (using (3)) it shows 2.5 (5/2) redundant TSVs. Whereas, four of the five cells cannot gain any benefit from the four redundant TSVs concentrated on one cell. Therefore, efficient distribution of signals can improve the overall effective redundancy, which in turn improves yield. To illustrate this phenomenon, let us consider the same example, i.e., if 5 signals have to be transferred across the two tiers through 1:4 TSV cells. Equation (1) shows that two such cells are required. The distribution of the TSV signals can take any of the following two possibilities: 1. One of the cells contains four TSV signals (1 redundant TSV) and other cell carries one TSV signal (4 redundant TSVs) 2. One of the cells with three TSV signals (2 redundant TSVs) and the other cell contains two signal TSVs (3 redundant TSVs). So we propose to obtain the effective Red_I/cell by summing the multiplication of redundant and signal TSVs for each cell and average it out over the number of signals transferred (X). Mathematically, it can be represented as follows:

$$\textit{Effective } Red_I/Cell = \frac{\sum_{i=1}^{N}(Red_i \times Sig_i)}{Total\_signal\_TSVs} \tag{4}$$

To elaborate on (4), effective Red_I/cell is computed for the above case as follows. For first possibility: Effective Red_I/cell = (1×4+ 4×1)/5 = 1.6. Similarly, the second possibility leads to: Effective Red_I/cell=(2×3+3×2)/5 = 2.4, This example shows that although average Red_I/cell (using (3)) is the same for both the examples, but a well spread out redundancy (more than 1 redundant TSVs in both cells in the second example) leads to effective Red_I/Cell. Substituting Red_I from (2) into (4) leads to (5). Practically, (5) is based on the assumption that failed TSV signal can be re-routed to any redundant TSV.

$$\textit{Effective } Red_I/Cell = \frac{\sum_{i=1}^{N}((5-Y_i) \times Y_i)}{Total\_signal\_TSVs} \tag{5}$$

B. 2:4 TSV Redundancy:

The 2:4 TSV redundancy technique, as shown in Fig 2(b), can tolerate up to two failures. This standard cell is identical to 1:4 cell except for number of redundant TSVs. Red_I can be found by using (6).

$$Red_I = 6 - Y \tag{6}$$

Similar analysis, as done for the case of 1:4 TSV cell, leads to the following equation for effective Red_I/cell:

$$\textit{Effective } Red_I/Cell = \frac{\sum_{i=1}^{N}((6-Y_i) \times Y_i)}{Total\_signal\_TSVs} \tag{7}$$

$$\textit{Where } N=\left\lceil \frac{X}{4} \right\rceil \text{ (given by (1))}$$

C. Router Based Redundancy:

Generalization of router based TSV cell requirement (shown in Fig. 2(c)) can be made as follows. It is considered that there are X signals that need to traverse from tier 1 to tier 2, using a router based redundant TSV cell, as shown in Fig. 2(c). Based on the above two parameters, Equation (8) can provide the number of router-based redundant TSV cells.

$$\textit{Router-based Cell Required} = N = \left\lceil \frac{X}{p \times q} \right\rceil \quad (8)$$

For Y number of signal TSVs, being used in a cell to transfer signals in a particular p×q cell, the redundant TSVs in each cell can be written as (9). Maximum p×q signals can be sent through one cell and it contains p+q redundant TSVs.

$$Red_l = [(p \times q) - Y] + (p + q) \quad (9)$$

If Y_i signals transfer through ith cell as an example, we can calculate effective Red_l/cell of each possible combination by expanding (4) based upon router based cell parameters. Physically, it has been assumed that each failed TSV path can be re-routed to any unused TSV. It can be written as follows:

$$\textit{Effective } Red_l/Cell = \frac{\sum_{i=1}^{N}[((p \times q) - Y_i) + (p+q)] \times Y_i}{Total\_signal\_TSVs} \quad (10)$$

$$\textit{Where } N = \left\lceil \frac{X}{p \times q} \right\rceil \text{ (given by (8))}$$

IV. Analysis of Effective TSV Redundancy Against Hardware Overhead

Simulation of three TSV redundancy techniques, mentioned in Section II and analyzed in Section III, is performed using MATLAB 7.0. We analyzed the hardware overhead required for each redundancy up-to 400 signals. Fig. 3 illustrates product of hardware with the number of cells used, using 1:4, 2:4 and router based TSV redundancy techniques. In order to provide a fair comparison, we normalized the product of number of cells and area overhead (called as hardware overhead) for a 5x5 router based redundancy technique over 400 signals.

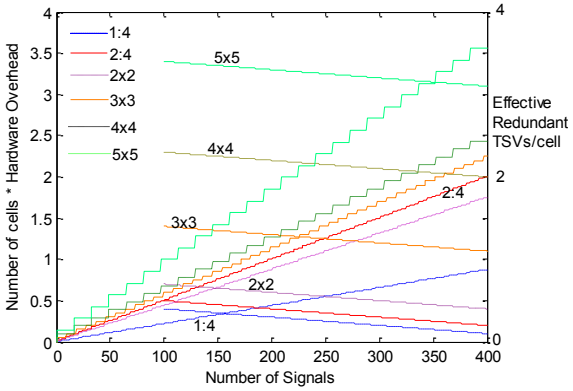


Figure 3. Hardware overhead X cells required (on left y-axis) and effective number of redundant TSVs (on right y-axis) for different number of signals

Fig. 3 shows that as expected, with an increment in the number of signals hardware overhead increases. However, effective redundancy per cell is reduced with an increment in the number of signals. It can be seen that the effective redundancy of router based TSVs is better at the expense of added hardware. Nonetheless, for 250 signals, the hardware overhead for 3x3 router based technique is about 3 times more than 1:4 redundancy technique, while providing 5 times more effective redundancy per cell. Hence, if the foundry data is available with respect to yield percentage of TSVs, this study will help the designer to choose the right redundancy technique under a given condition.

V. Case Study: CDC in 3-D ICs

The CDC technique is gaining its importance in 3-D IC as the multiple logic-tiers of 3-D ICs need to communicate with each other. As a case study in this paper we considered two CDC techniques: semi QDI based GALS design and loosely synchronous interface design. Semi Quasi Delay insensitive (semi-QDI) based GALS design uses different codes that embed control signals in data signals [11]. One-of-N, dual rail and m-of-n encoding are majorly used in these designs mainly due to their simplicity [11]. One-of-N encoding requires 2^N bits for N bit data. Dual rail requires two bits to encode a single bit, whereas ${}^{m}C_n$ values can be encoded through m-of-n encoding, for further elaboration on DI encoding technique please refer to [11][12]. For the case study, we implemented semi QDI based GALS design, as shown in Fig. 4, which is using 1-of-N encoding technique.

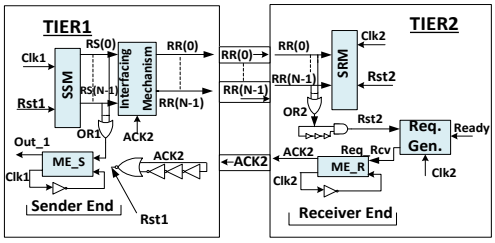


Figure 4. Architecture of QDI based GALS CDC technique in 3-D IC

To further extend the results, a representative circuit of another class of CDC technique is implemented, which is called loosely synchronous, because of its utilization of timing assumptions. The representative interface is depicted in Fig. 5, where it is shown that two control signals along with one clock signal are required for CDC.

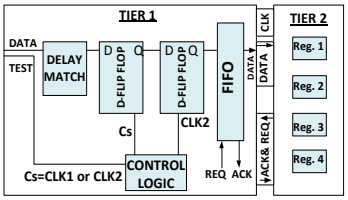


Figure 5. Loosely synchronous interface architecture for CDC in 3-D IC

This example circuit is called self-tested self-synchronization (STSS) circuit [12] [13] for studying CDC implementation in 3-D ICs. For both CDC techniques, the transfer of four data signals is considered in our simulation.

TSV Requirements: For semi QDI based GALS design, 16 data signals are required to transfer four data bits, when 1-of-N encoding is used with one ACK signal (control signal). So, in total 17 TSVs are required, as stated in row 1 of Table I.

Table I. TSVs required for CDC Techniques (Four Bit Data Transfer)

Semi QDI Based GALS				**Loosely Synchronous (STSS)**
Redundancy	*1-of-N Encoding*	*3-of-6 Encoding*	*Dual rail Encoding*	*No Encoding*
No Redundancy	17	7	9	7
1:4 TSV Redundancy [7]	25	10	15	10
2:4 TSV Redundancy [8]	30	12	18	12
Router based Redundancy[9]	30	15	15	15

In a similar way, 3-of-6 encoding has 3 asserted signals out of 6 signals. Transport of four bits using 3-of-6 encoding requires six data signals and one control signal (row 1 column 2 in Table I). For dual rail encoding, each bit is encoded into two bits. Therefore, overall eight signals for data and one control signal are required to transfer four bits of data.

Table I shows that STSS based technique and 3-of-6 encoding technique require least number of TSVs to transfer four data bits. Hence, this analysis can utilize the graph, shown in Fig. 3 to provide the designer a first-order design choice among different TSV-redundancy techniques.

From Table II, we know the number of TSVs required, required number of cells, average number of redundant TSVs per cell and effective *Red$_f$/cell* for each redundancy type. Effective Red$_f$/Cell column for 1-of-N encoding and dual rail shows three different values for each redundancy case. This is due to the fact that there are three different possibilities to spread the TSVs in different cells in order to achieve better effective Red$_f$/cell.For example, the case of 1-of-N encoding 17 signals can pass across tiers using 1:4 TSV redundancy. The three options can be as follows: Opt.1. Four cells with four signals and one cell with one signal. Opt.2. Two cells with four and three cells with three signals. Opt.3. Three cells with four signals, one cell with three and one cell with two signals. Each option has different effective *Red$_f$/cell* values, 1.18, 1.53 and 1.41, for opt. 1, opt. 2, and opt. 3, respectively,

VI. CONCLUSION

In this paper inter-logic layer communication issues related to yield aware perspective are addressed. Various yield improving TSV redundancy techniques have been analyzed. Closed form mathematical equations are formulated to facilitate the 3-D IC designers to make informed decision in choosing yield enhancing TSV redundancy techniques. The utilization of our proposed yield aware design suggestion methods is illustrated with a case study on CDC techniques.

Table II. TSV statistics using three redundancy techniques

Semi QDI Based GALS Interface										**Loosely Synchronous Interface (STSS)**		
Redundancy	*1-of-N Encoding*			*3-of-6 Encoding*			*Dual rail Encoding*			*No Encoding*		
	Cell used	*Average Red$_f$/cell*	*Effective Red$_f$/cell*	*Cell used*	*Average Red$_f$/cell*	*Effective Red$_f$/cell*	*Cell used*	*Average Red$_f$/cell*	*Effective Red$_f$/cell*	*Cell used*	*Average Red$_f$/cell*	*Effective Red$_f$/cell*
Redundancy 1:4 [7]	5	1.6	(opt.1)1.18 (opt.2)1.53 (opt.3)1.41	2	1.5	(opt.1) 1.5	3	2	(opt.1)1.33 (opt.2)1.78 (opt.3) 2	2	1.5	(opt.1) 1.5
Redundancy 2:4 [8]	5	2.6	(opt.1)2.18 (opt.2)2.53 (opt.3)2.41	2	2.5	(opt.1) 2.5	3	3	(opt.1)2.33 (opt.2)2.78 (opt.3) 3	2	1.5	(opt.1) 1.5
Redundancy Routers [9]	2	6.5	(opt.1) 6.5	1	8	(opt.1) 8	1	6	(opt.1) 6	1	8	(opt.1) 8

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