Clock Domain Crossing (CDC) for Inter-logic-layer Communication in 3-D ICs

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***Abstract*—3D technology is becoming more popular due to improved design density and performance. Besides this, single global clock distribution to a complex system like 3-D IC is very challenging. Due to potentially heterogeneous, dice integration also omens for increasing environmental and process non-idealities. Therefore, inter-logic layer communication in 3-D ICs can leverage from clock domain crossing (CDC) techniques to perform timely and correct data transactions. In this paper, we investigate the two classes of CDC techniques, the delay insensitive (DI) based GALS and loosely synchronous CDC technique under 3-D IC context. It is found that although DI based GALS designs are attractive solution because of the relaxed constraint on clock distribution network, but for 8 data-bits/transaction or higher its hardware overhead becomes more than the counterpart loosely synchronous design. To the best of authors' knowledge this is a premier work in investigating design guidelines for CDC techniques in through silicon via based 3-D ICs .**

Keywords— GALS, 3-D ICs, Clock Domain Crossing, TSV

I. INTRODUCTION

3-D IC technology has recently emerged as a solution to the interconnect bandwidth bottleneck in conventional 2-D ICs. The multi-layer structure in 3-D IC provides advantages in form of reduced wire length, less delay, low power consumptions and improved performance density over their counterpart 2-D ICs [1]. It is envisaged that future 3-D ICs require integration of heterogeneous dice, with each of them may even from different vendors. This leads to the realization of multiple clock domains (MCDs) [2] [3], which require clock domain crossing (CDC) interfaces. Due to peculiar characteristics of 3-D ICs, it lead to realization of globally asynchronous and locally synchronous (GALS) [4] circuits incorporation into 3-D IC.

This paper investigates various challenges associated with the incorporation of two widely used CDC techniques, asynchronous based and loosely synchronous based, into 3-D ICs. The representative interfaces used for simulations are DI-based GALS design for the first class of CDC techniques and self-test self-synchronization (STSS) circuit [5] for the second class of CDC technique. Based upon proof of concept electrical simulations, design guidelines are extracted to achieve lesser footprint against TSV requirements. For hardware overhead, it is found out that if 8 or more data bits needs to be transferred per data transaction then STSS based loosely synchronous CDC technique requires lesser footprint compared to DI based GALS designs. Performance wise DI based CDC is marginally better.

Rest of the paper is organized as follows; Section II presents the background required to understand this work. Section III describes inter-logic layer communication fomenter-logic layer communication from 3-D IC design perspective. Section IV presents electrical simulation results for two CDC implementations. Finally, Section V concludes this paper.

II. BACKGROUND

A. Clock Domain Crossing Techniques

CDC Interface can be broadly categorized as asynchronous or loosely synchronous. First, category of asynchronous interfaces uses delay insensitive (DI) protocols, which depends on data encoding techniques. Due to low complexity in encoding and decoding [6], 1-of-N and dual rail data codes (explained later) are used mostly to implement DI protocols. Other data encodings such as m-of-n codes, are efficient in terms number of bits/data, but are more complex to implement. One-of-N encoding is like one-hot or cold encoding that has one bit asserted at a time. For N-bit data, 2^N wires are required to transmit these binary values. Hence, number of wires increases exponentially (2^N) with the number of bits. Table I illustrates 1-of-4 encoding as an example of 1-of-N encoding.

TABLE I. 1-of-4 ENCODING (AN EXAMPLE OF 1-of-N ENCODING)

Two bit value	1-of-4 encoding			
00	0	0	0	1
01	0	0	1	0
10	0	1	0	0
11	1	0	0	0

On the other hand, dual rail encoding requires two signals to encode a single bit of data. For example, for 8-bit data, 16 signals are required to encode it. Second, class of CDC techniques utilizes loosely synchronous interfacing mechanisms that help in resolving the metastability using synchronization mechanisms. In such interfaces, a phase detection mechanism detects the phase of the incoming data

and adjusts the local clock signal (or its phase) to avoid any metastability [5].

B. 3-D IC Using TSVs

In 3-D ICs, different tiers are stacked vertically and they need to communicate. Special vertical interconnects, called as through silicon via (TSV), are used for this communication purpose. Fig. 1(a) is a conceptual illustration of TSVs between two different tiers. Fig. 1(b) is the associated π electrical model of TSV as used in the reference [7].

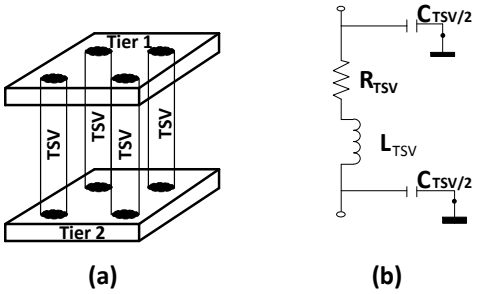

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Fig. 1. a) TSVs in 3-D ICs b) Electrical model of TSV

III. INTER LOGIC LAYAER COMMUNICATION IN 3-D IC

A. DI Based GALS Technique For 3-D ICs

This section provides full design details of the proposed implementation of CDC technique for 3-D ICs, which uses DI-based GALS design. Fig. 2 shows one such implementation. This CDC technique is spread across two communicating logic-tiers as shown in Fig. 2. At tier 1, the synchronous sending module (SSM) sends out the encoded data signals (RS (0) to RS (N-1)) through an asynchronous DI interface. In this work, the DI based interface is implemented using 1-of-4 data encoding technique as described in preceding section (Section II). One-of-4 encoding can be implemented using various asynchronous interfaces [8], [9]. The asynchronous switching interface on tier 1 takes data from SSM and passes it on to tier 2. ACK2 signal acts as an enable/disable switch for the interface. On tier 2, the data (RR (0) to RR (N-1)), is received by synchronous receiving module (SRM)**.** ME_S and ME_R, at tier 1 and tier 2 respectively, are mutually exclusive elements, which control their respective Clk1 and Clk2 signals. Req_Gen block is based on true single phase clocking register (TSPCR)) to pass the ready signal from receiver side.

1) Sequence of Signals: From 3-D perspective, SSM and interfacing mechanism along with ME_S and ring oscillators are placed on tier 1 while SRM along with ME_R, Req_Gen blocks and ring oscillator are on tier 2. Such a placement is chosen to reduce the TSV footprint, as it requires TSV for encoded data signals (using return-to-zero (RTZ) signaling protocol) and ACK2 signals only. Waveform illustration for the DI based GALS technique for CDC is provided in Fig. 3.

To understand the working of the interface, sequence of events is described as follows:

a) Initial Requirement: Initially, at tier 1 all signals are considered at logic zero, due to the implementation of RTZ signaling protocols.

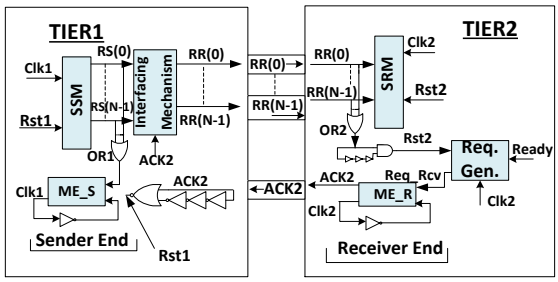


Fig. 2. DI based GALS CDC Architecture in 3-D IC

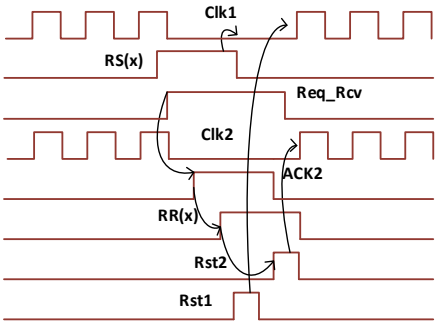


Fig. 3. Operation of DI based GALS CDC technique using DI protocol

b) Data Transfer: i. When RS(x) signal is asserted, here x could be any number from 0 to (N-1) and N is the total number of signal lines (shown in Fig. 2 at tier 1), it stops the Clk1 signal through ME_S element.

ii. On the other end of the interface, at tier 2, the Clk2 stops when Req_Rcv signal is asserted via ready signal. This in turn sends the ACK2 signal to tier1 indicating that the receiver is ready to receive data. Prior to the assertion of ACK2, sender could not send data.

iii. ACK2 signal assertion enables the switching interface and data goes through this interface to SRM in the form of (RR(x)) signal.

c) Data Completion: i. Data completion on SRM leads to the generation of Rst2 pulse which brings the Req_Rcv signal down and releases Clk2.

ii. Rst1 pulse, which is generated as soon as the completion of data is acknowledged via ACK2 signal, allows the Clk1 to restart.

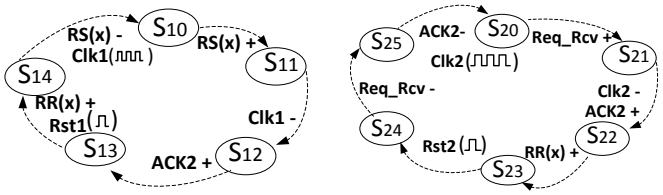
Number of TSVs for data signals RR(x) is not affected by switching interface placement on tier2 or on tier1. For control signals, if switching interface is placed on tier2, ACK2 signal is considered to be local to that tier. Now, instead of ACK2, Rst1 will have to pass through TSV. But number of TSVs will remain same. As only one control signal pass through TSV.

2) State Transition Graphs (STG): To understand the working of each tier separately, two state transition graphs are provided in Fig. 4.

a) Tier 1 STG: S_{10} is the idle state where all the control signals at tier 1 are at zero level, and Clk1 runs freely (SSM works normally). S_{10} to S_{11} transition shows that the data transfer begins, RS(x) is asserted i.e. the data is asserted to pass through the asynchronous interface. Next, S_{11} to S_{12} transition indicates that the sender tier has stopped (Clk1 has

paused). S_{12} to S_{13} transition shows triggering of asynchronous interface to transfer data, courtesy to the assertion of ACK2 signal. With S_{13} to S_{14} transition, completion of data transaction begins. Due to ACK2 signal assertion the RR(x) signal is asserted and Rst1 pulse is generated. During S_{14} to S_{10} transition tier 1 returns back to its idle state, with resetting the RS(x) data signals and releasing the Clk1 signal.

b) Tier 2 STG: S_{20} represents an idle state, where all signal are at zero level till the request for data is received. Clk2 runs freely and SRM works normally at Clk2 signal frequency. State S_{20} to S_{21} transition at tier 2 indicates that request for data (Req_Rcv) has been received which is an indication of SRM receiving mode. State transition occurs from S_{21} to S_{22} when ACK2 signal gets asserted because of Req_Rcv assertion, and it (Req_Rcv) also pauses the Clk2 signal. S_{22} to S_{23} transition is caused by the assertion of RR(x) signal that is the corresponding receiver side signal of sender data (RS(x)) via asynchronous switching interface). S_{23} to S_{24} state transition indicates that receiver has received the data (RR(x)), and Rst2 pulse is generated. S_{24} to S_{25} transition shows the beginning of completion of the data transaction, as Rst2 pulse results in negation of Req_Rcv signal. S_{25} to S_{20} transition indicates the completion of data transaction, after the negation of Req_Rcv, ACK2 & Clk2 signals.



4(a) Tier 1 signals transitions 4(b) Tier 2 signals transitions

Fig. 4. Operation of DI based GALS CDC technique on state transition graph

B. STSS [5] CDC Technique For 3-D IC

In this section we elaborate another class of CDC, which is loosely synchronous technique. To do the interlayer communication in 3-D IC, a well known class of loosely synchronous CDC technique, as already mentioned in Section II, the self-tested self-synchronization (STSS) is used. Fig. 5 shows the CDC implementation using STSS [5].

It is observed that the number of signals pass through TSV are unaffected by the fact that at which tier STSS based loosely synchronous CDC is implemented. Because, in this interface the only difference occurs due to STSS interface placement is the change in the directions of REQ and ACK signals (Fig. 5).

1) Sequence of Signals: STSS based loosely synchronous CDC operation is illustrated in Fig. 6 with the help of waveforms; the arrows represent causality among the signals. Similar to DI based GALS, the STSS based loosely synchronous CDC is also explained based on a pull channel, i.e. request (REQ) is initiated from the receiver, which is on tier 2 in this case as shown in Fig. 5. In response, the sender at tier 1 asserts the ACK signal and sends the data. On tier 2 data is received and ACK is negated, which represents that the data has been received.

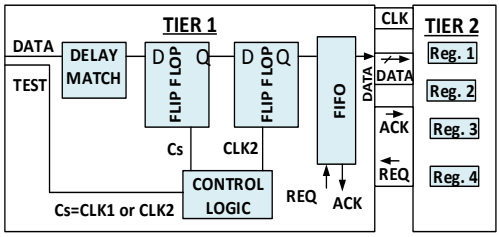


Fig. 5. Architecture of modified STSS based loosely synchronous CDC technique for 3-D ICs

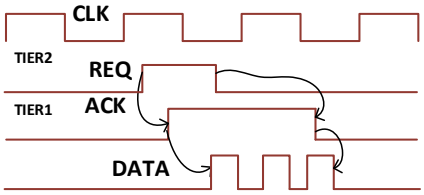


Fig. 6. Operation of STSS based loosely synchronous CDC technique in 3-D environment

2) State Transition Graphs (STG): Fig. 7 is the description of protocol using states transition graph for the whole system shown in Fig. 5.

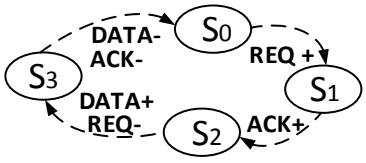


Fig. 7. STSS based loosely synchronous CDC technique operation through STG.

When REQ is asserted state transition occurs between S_0 to S_1. When sender acknowledges the request by asserting ACK signal, it leads to transition from state S_1 to S_2. Receiver negates the REQ and sender puts data on the data line, and the sender transits from state S_2 to S_3. After the completion of data transfer, system is brought back to idle state S_0, with the negation of ACK and DATA signals.

IV. Simulation Results

Both CDC techniques, DI based GALS and STSS based loosely synchronous, are simulated in Cadence 90nm technology using IHP microelectronics libraries. For DI based GALS CDC, GAsP asynchronous interface [8] has been used as switching mechanism for simulation purposes. Electrical model of TSV [7] based upon analytical method, used across different tiers (Fig. 1b). In our case, RLC values used were based on model of TSV which is 6um in diameter, 20um in length, with oxide thickness of 120nm and with 10um pitch distance. Using the state of art empirical analysis based model from reference [10] following parasitic values are obtained R=12.89 mΩ, C=9.807 fF and L=5.816 pH respectively.

Table II indicates that area wise, DI based GALS design has advantage over STSS for lower number of bits, but as we increase the number of bits STSS becomes more suitable. For example if 1-bit is transferred STSS uses 1.44 times more area compared to DI based GALS. However, if 16 bit data

transaction is made concurrently, DI based GALS consumes about 1.14 times STSS technique (row 4 of Table II).

TABLE II. HARDWARE OVERHEAD OF CDC TECHNIQUES

Case	STSS [5]based CDC			DI based GALS CDC		
	PMOS	*NMOS*	*Total*	*PMOS*	*NMOS*	*Total*
1-bit	1.37X1	1.66Y1	1.44T1	X1	Y1	T1
4-bit	1.12X2	1.25Y2	1.16T2	X2	Y2	T2
8-bit	X3	1.07Y3	T3	1.25X3	Y3	1.15T3
16-bit	X4	Y4	T4	1.19X4	1.03Y4	1.14T4

Table III shows number of TSVs required for different number of bits transfer across tiers. DI based GALS uses different DI encoding as described in Section II. It can be seen that only for 1-bit case it has lower TSV footprint, beyond 1-bit transfer STSS based loosely synchronous CDC is better.

TABLE III. TSV OVERHEAD FOR CDC TECHNIQUE

DI Based GALS CDC				STSS CDC
Case	*1-of-N Encoding*	*m-of-n Encoding*	*Dual rail Encoding*	*No Encoding*
1-bit	3	3	3	4
4-bit	17	9	9	7
8-bit	257	17	17	11
16-bit	65536	33	33	19

Fig. 8 shows simulation of DI based GALS according to protocol mentioned in section III. We obtained a maximum frequency of about 1.2GHz at tier2 and 500MHz at tier1.

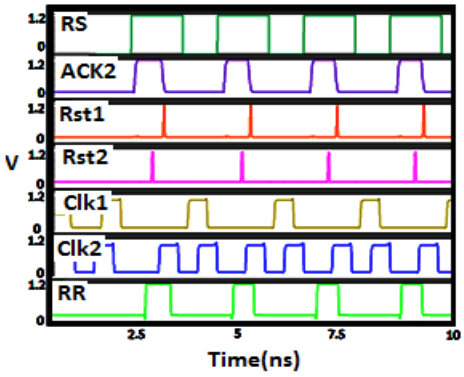


Fig. 8. Simulation results of DI based GALS CDC in 3-D IC.

Fig. 9 shows the simulation of STSS based loosely synchronous CDC technique, based on the protocol explained in section III (B) and on parameters described above in the same section. Due to the limitations of synchronization delay, it operates at frequency of 500MHz.

Table IV shows, power, energy and delay for both CDC techniques and it shows that there is very little difference between these two when it comes to energy-delay product, however DI based GALS CDC technique is marginally better.

V. CONCLUSION AND FUTURE WORK

This work provides an insight to the inter-logic-layer communication in 3-D ICs. Challenges of using some of the CDC techniques from 3-D IC perspective are identified. Various variants of two classes of CDC solutions i.e. DI based GALS and STSS based loosely synchronous are analyzed with respect to design choices. Metric analysis based on proof of concept simulation showed that performance and energy-delay product for both the design are comparable. Our analysis is a step towards developing design guidelines for inter-layer communication in 3-D IC designs. To the best of authors knowledge this is a premier work in investigating design guidelines for CDC techniques in TSV based 3-D ICs.

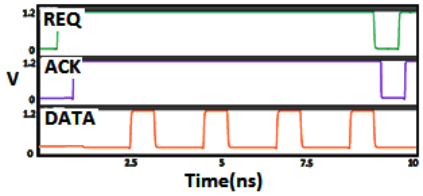


Fig. 9. Simulation results of modified STSS based CDC in 3-D IC.

Table IV. POWER, ENERGY and DELAY PRODUCT FOR 4-BIT DATA

S. No	Attribute	DI-based GALS CDC	CDC using STSS [5]
1	Power	2.75 mW	2.78 mW
2	Energy	14.17 mj	10.51 mj
3	Delay	.75 ns	1.03 ns
4	Power–Delay-Product	2.06 pWs	2.86 pWs
5	Energy-Delay-Product	10.63 pjs	10.82 pjs

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